Random Access Memory (RAM)

EED2003 Digital Design

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Overview

- **Memory is a collection of storage cells with associated input and output circuitry**
  - **Possible to read and write cells**
- **Random access memory RAM stores data temporarily**
- **RAM contains words of information**
- **Memory cells can be accessed to transfer information to or from any desired location with the same time regardless of the location.**
- **In contrast, in serial memories (magnetic disk or tape), takes different lengths of time to access the information, depending on where the desired location is relative to the current position of the disk or tape.**

Preliminaries

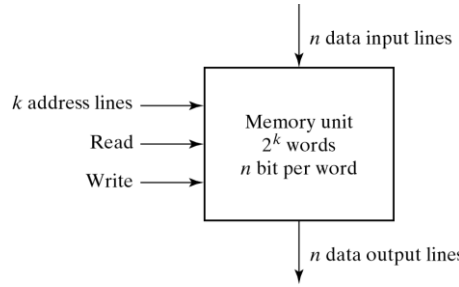
- **RAMs contain a collection of data bytes**
  - **A collection of bytes is called a word**
  - **Capacity of RAM device is usually described in bytes (e.g. 16 MB)**
- **Write operations write data to specific words**
- **Read operations read data from specific words**
- **Array logic symbols for gates**

(a) Conventional symbol (b) Array logic symbol

Fig. 7-1 Conventional and Array Logic Diagrams for OR Gate

RAM Interface Signals

- **Data input and output lines carry data**
- **Memory contains 2^k words**
  - **k address lines select one word out of 2^k**
- **Read *asserted* when data to be transferred to output**
- **Write *asserted* when data input to be stored**



Random-Access Memory (RAM)

Example: a memory unit w/ 1K words of 16 bits each

- **1024 x 2 bytes = 2K bytes**
- **decimal address: 0 to 1023**
- **address: 10 bits; data: 16 bits**

Memory address		
Binary	Decimal	Memory contents
0000000000	0	10110101 01011100
0000000001	1	10101011 10001001
0000000010	2	00001101 01000110
	⋮	⋮
1111111101	1021	10011101 00010101
1111111110	1022	00001101 00011110
1111111111	1023	11011110 00100100

RAM Size

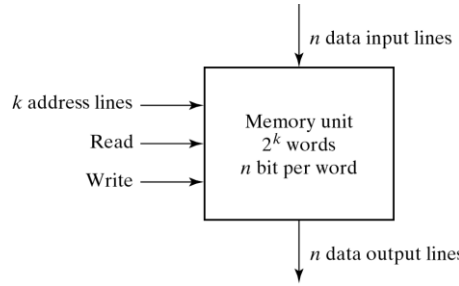
- **If memory has 2^k words, k address bits are needed**
  - **2^3 words, 3 address bits**
- **Address locations are labelled 0 to 2^k-1**
- **Common subscripts:**
  - **Kilo – 2^{10}**
  - **Mega – 2^{20}**
  - **Giga - 2^{30}**

Memory address		
Binary	decimal	Memory contest
0000000000	0	1011010101011101
0000000001	1	1010101110001001
0000000010	2	0000110101000110
	⋮	⋮
1111111101	1021	1001110100010100
1111111110	1022	0000110100011110
1111111111	1023	1101111000100101

Content of a 1024 × 16 Memory

Write Operation

1. **Apply binary address of word to address lines**
2. **Apply data bits to data input lines**
3. **Activate write input**



Block Diagram of a Memory Unit

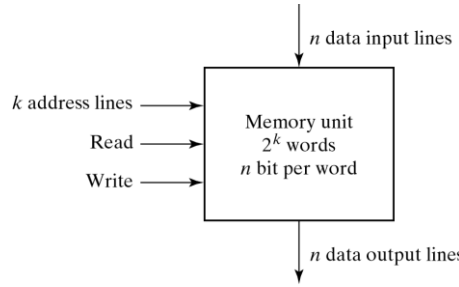
Data output lines unused

Read input signal should be inactive

Delay associated with write

Read Operation

1. **Apply binary address of word to address lines**
2. **Activate read input**



Block Diagram of a Memory Unit

Data input lines unused
Write input signal should be inactive

Delay associated with read

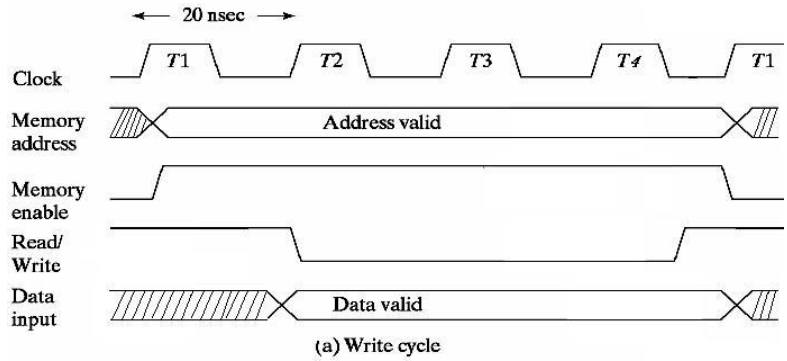
Memory enable used to allow read and writes

Memory Timing - write operation

Memory does not use a clock

- **Control signals may be generated on clock edges**

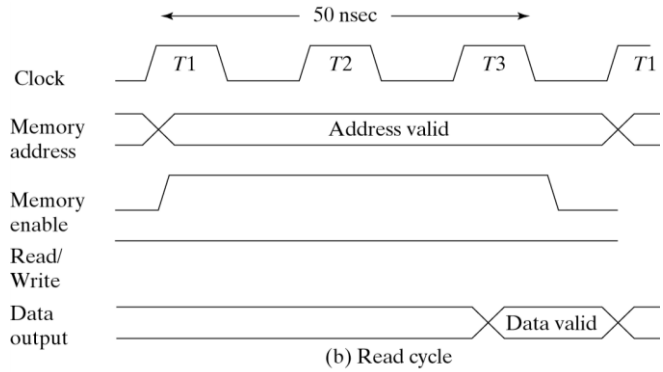
- **Cycle time is the maximum time from the application of the address to the completion of the operation to store the data.**



(a) Write cycle

Timing Waveforms – read operation

- **Access time indicates time to read**
- **Address indicates location**
- **Data valid on Data Output following access time**



(b) Read cycle

Multiple clock signals needed for data read in this example

Types of Random Access Memories

- **Static random access memory (SRAM)**
  - **Operates like a collection of latches**
  - **Once value is written, it is guaranteed to remain in the memory as long as power is applied. Since it doesn't need refresh, static RAM's power consumption is much less than dynamic RAM.**
  - **Static RAM cells use 4-6 transistors to store a single bit of data. This provides faster access times at the expense of lower bit densities.**
  - **Generally expensive**
  - **Used inside processors (like the Pentium)**
  - **Extensively for second level cache memory, where its speed is needed and a relatively small memory will lead to a significant increase in performance. A high-performance 1998 processor will generally have 512kB to 4Mbyte of L2 cache.**

Types of Random Access Memories

- **Dynamic random access memory (DRAM)**
  - **Generally, simpler internal design than SRAM**
  - **Requires data to be rewritten (refreshed), otherwise data is lost**
  - **Often hold larger amount of data than SRAM**
  - **Longer access times than SRAM**
  - **Used as main memory in computer systems**

Inside the RAM Device

- Address inputs go into decoder
  - Only one output active
- Word line selects a row of bits (word)
- Data passes through OR gate
- Each binary cell (BC) stores one bit
- Input data stored if Read/Write is 0
- Output data driven if Read/Write is 1

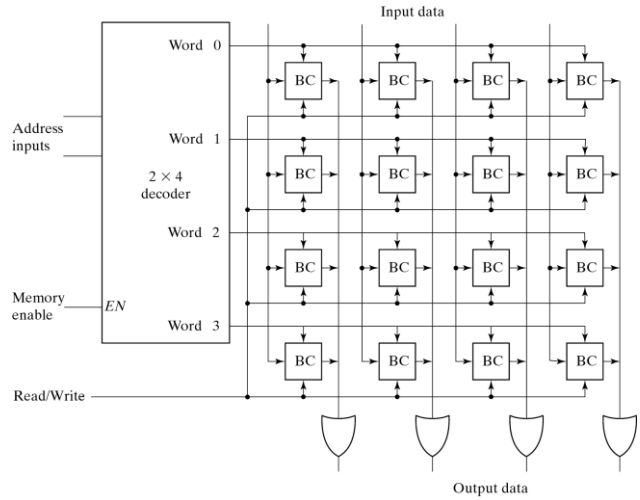
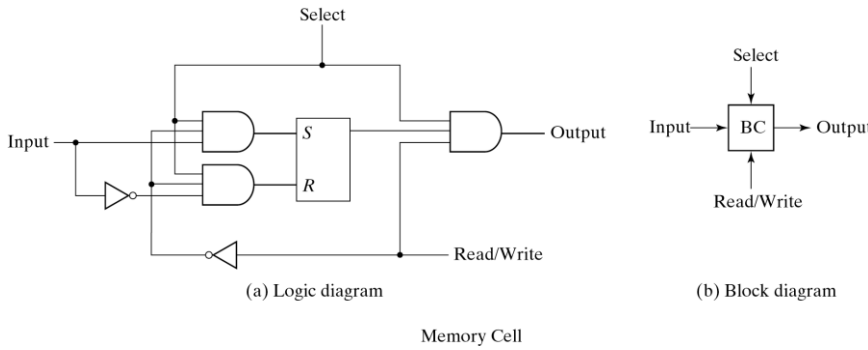


Fig. 7-6 Diagram of a 4 × 4 RAM

Inside the SRAM Device

- Basis of each SRAM cell is an S-R latch
- Note that data goes to both S and R
- Select enables operation
- Read/write enables read or write, but not both



Memory Cell

Inside the SRAM Device

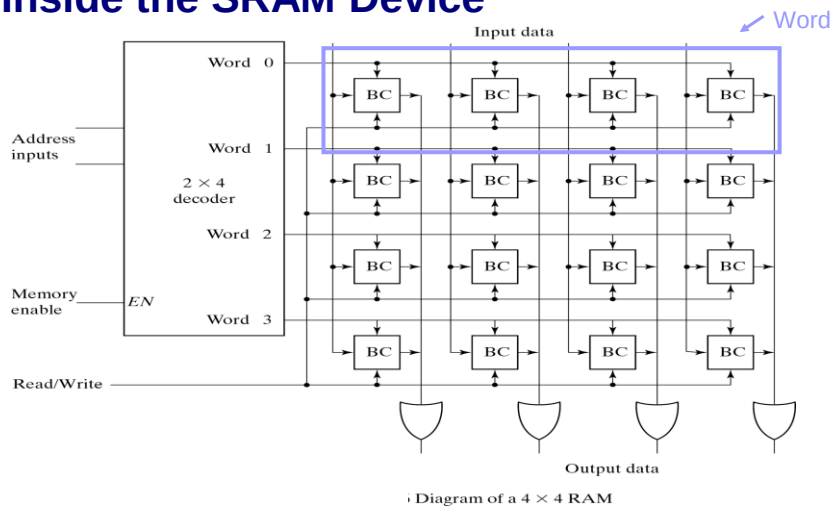
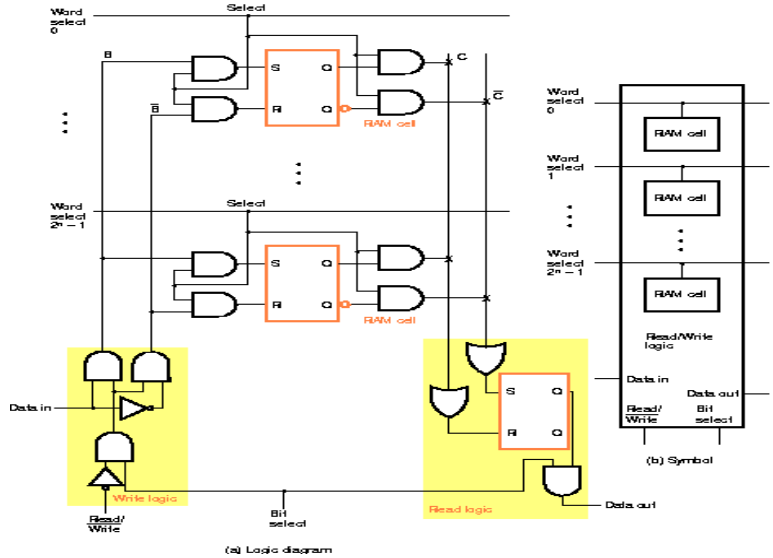


Diagram of a 4 × 4 RAM

- **Note:delay primarily depends on the number of words**
- **Delay not effected by size of words**

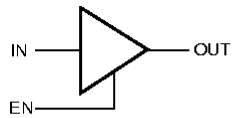
RAM Integrated Circuits

- **RAM Bit Slice Model**



Three-state Buffer

- have three distinct states
  - logic-0, logic-1, high-impedance (Hi-Z) state
  - Hi-Z state: open circuit,
    (the output appears to be disconnected)
- ENABLE input (*EN*)



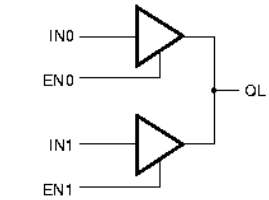
(a) Logic symbol

EN	IN	OUT
0	X	Hi-Z
1	0	0
1	1	1

(b) Truth table

Three-state Buffer

- Form a multiplexed output line



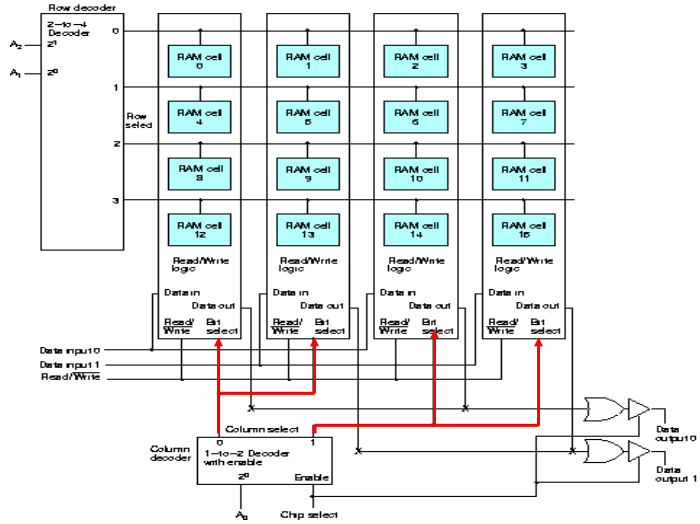
(a) Logic Diagram

EN1	EN0	IN1	IN0	OL
0	0	X	X	Hi-Z
(S) 0	(S') 1	X	0	0
0	1	X	1	1
1	0	0	X	0
1	0	1	X	1
1	1	0	0	0
1	1	1	1	1
1	1	0	1	
1	1	1	0	

(b) Truth table

truth table (in shaded area) is a 2-way multiplexer with S

8 x 2 RAM chip (8 words of 2 bits each)

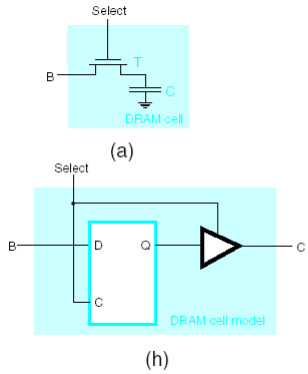


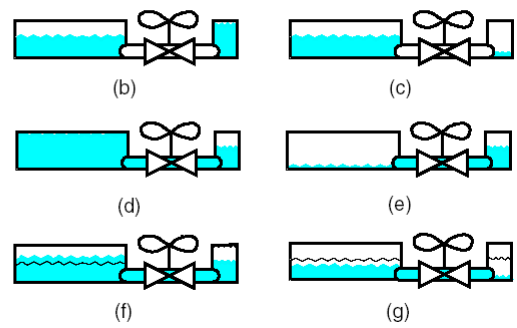
3 address bits: two are handled by the row decoder

column decoder has only one address bit & produces 2 column select lines

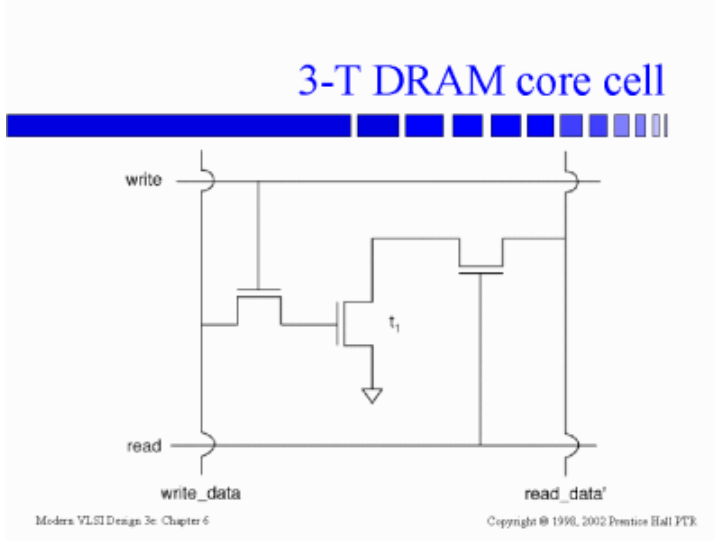
DRAM

- The transistor acts like a switch
- When the switch is closed, the charge can be flow from the bit value B to the capacitor C.
- When the swith is open, the value in the capacitor is stored.





Inside DRAM Cell



3-T DRAM operation

- Value is stored on gate capacitance of t_1.
- Read:
  - read = 1, write = 0, read_data' is precharged;
  - t_1 will pull down read_data' if 1 is stored.
- Write:
  - read = 0, write = 1, write_data = value;
  - guard transistor writes value onto gate capacitance.

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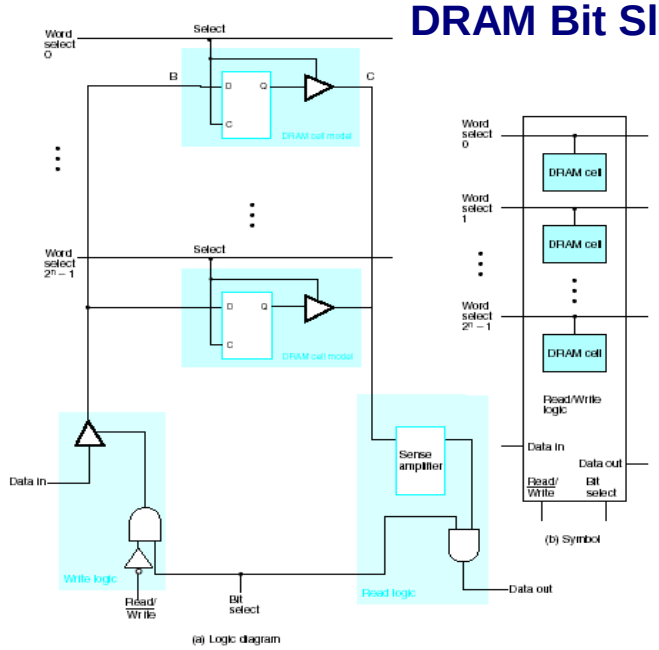
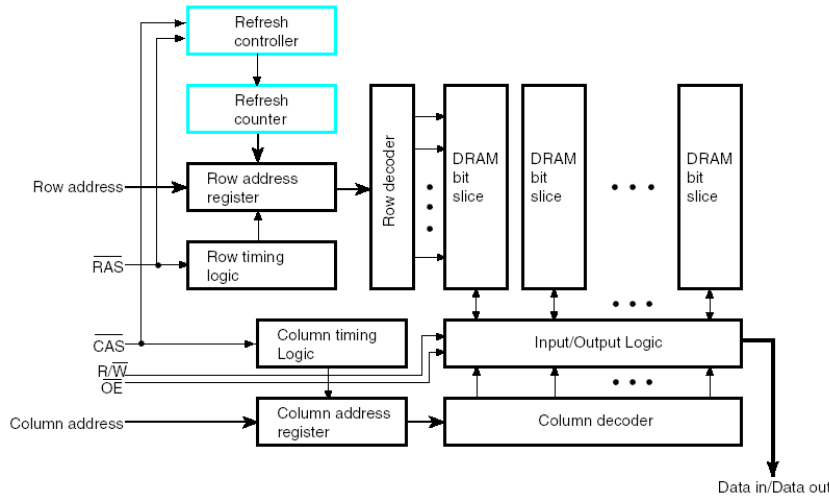
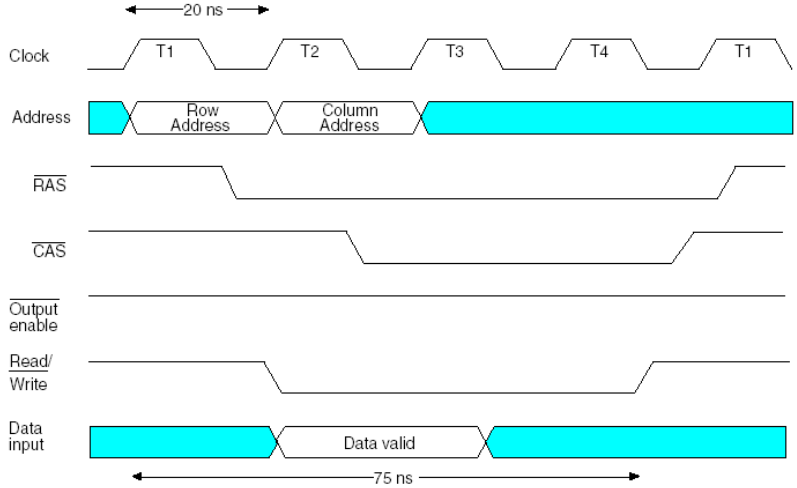
DRAM Bit Slice Model



Block diagram of a DRAM including Refresh Logic

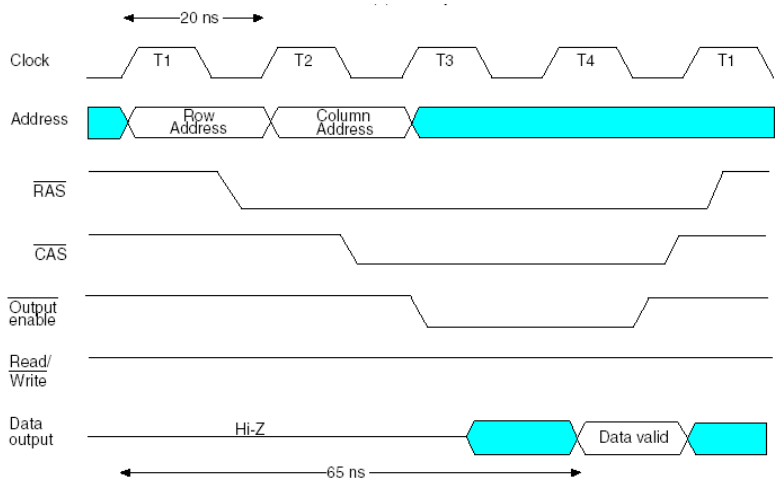


DRAM Write Timing



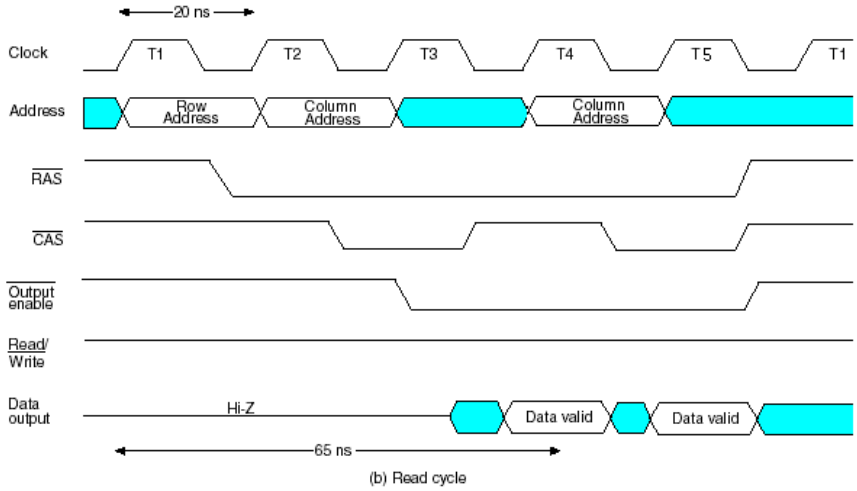
(a) Write cycle

DRAM Read Timing



(b) Read cycle

Page Mode

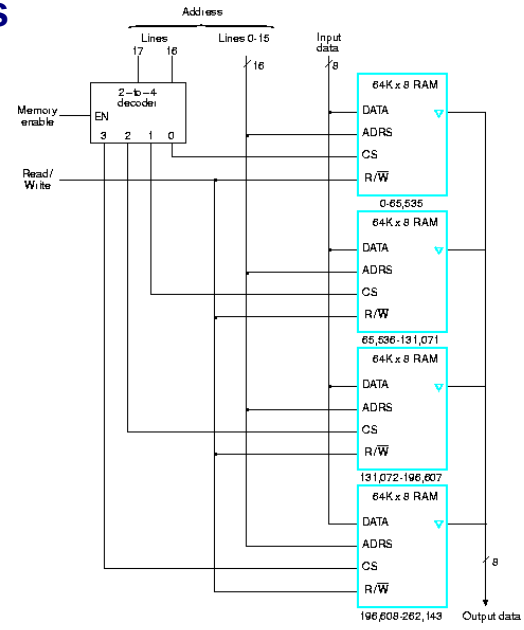


(b) Read cycle

Array of RAM ICs

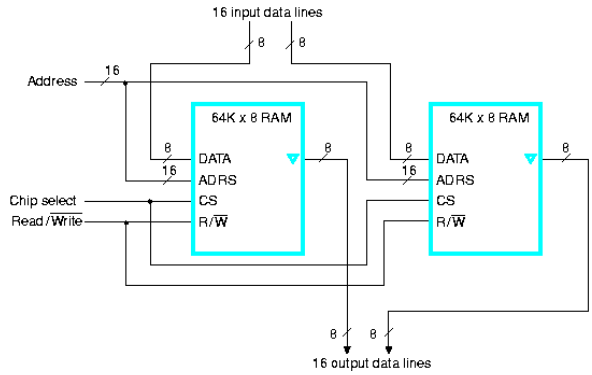
construct 256K x 8 RAM

- **four 64K x 8 RAM chips**
- **requires 18-bit address lines**
- **2 MSBs are applied to a 2 x 4 decoder,**
- **4 outputs are applied to the CS inputs of the four chips**



Array of RAM ICs

- Form a 64K x 16 memory
  - 16 data input & output lines are split between the two chips



Error Detection and Correction

- parity-bit
  - most common error-detection scheme
  - it is generated & stored along with data word in memory
  - checked after reading the word in memory
  - the data word is accepted if the parity is correct
  - the error cannot be corrected

- check-bits
  - an error-correcting code generates multiple check bits
  - each check bit is a group of bits in the data word
  - check bits compare with the stored parity;
    generate a unique pattern (*a syndrome*) to identify the bit in error

Error Detection and Correction

- Hamming Code
  - most common error-correcting codes used in RAM
  - k parity bits are added to an n-bit data word, forming n+k bits
  - positions as a power of 2 are reserved for the parity bits;
    the remaining bits are the data bits

(ex) 8-bit data word 11000100

Bit position 1 2 3 4 5 6 7 8 9 10 11 12

P_1 P_2 1 P_4 1 0 0 P_8 0 1 0 0

P_1 = XOR of bits (3,5,7,9,11) = 0

P_2 = XOR of bits (3,6,7,10,11) = 0

P_4 = XOR of bits (5,6,7,12) = 1

P_8 = XOR of bits (9,10,11,12) = 1

12-bit composite word = 0 0 1 1 1 0 0 1 0 1 0 0

Error Detection and Correction

(ex) Error

Bit position 1 2 3 4 5 6 7 8 9 10 11 12

0 0 1 1 1 0 0 1 0 1 0 0 No Error

1 0 1 1 1 0 0 1 0 1 0 0 Error in bit 1

0 0 1 1 0 0 0 1 0 1 0 0 Error in bit 5

C_8	C_4	C_2	C_1	
0	0	0	0	No Error
0	0	0	1	Error in bit 1
0	1	0	1	Error in bit 5

- Hamming code can be used for data words of any length
  n (data bits) & k (check bits) to accomodate a word of 2^k-1
  $n = 2^k - 1 - k$ (or less)
- can detect & correct only a single error

Summary

- Memories provide storage for computers
- Memories are organized in words
  - Selected by addresses
- SRAMs store data in latches
  - Accessed by surrounding circuitry
- RAM waveforms indicate the control signals needed for access
- Words in SRAMs are accessed with decoders
  - Only one word selected at a time
- Some staragеies have been developed for error correction.